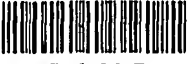
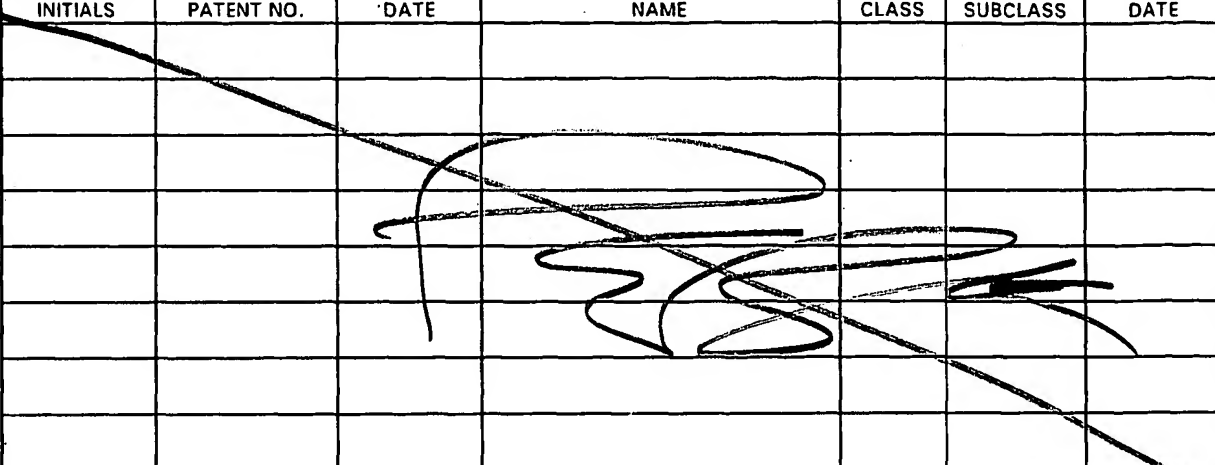
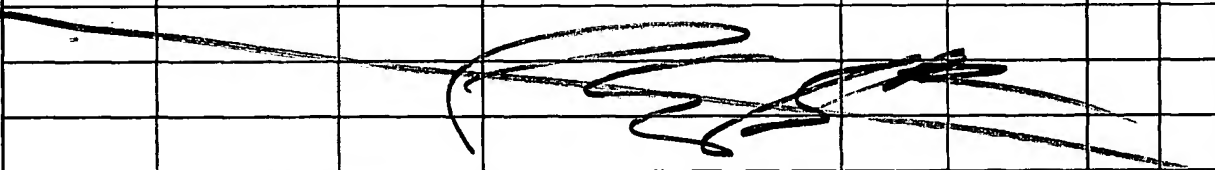


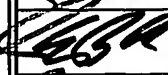






<b>INFORMATION DISCLOSURE CITATION</b> PTO-1449		 <b>26615</b> <small>PATENT TRADEMARK OFFICE</small>	ATTORNEY'S DKT No. H1132 APPLICANT(S) Ming-Ren Lin et al. FILING DATE July 8, 2003	APPLICATION No. <u>Unassigned</u> GROUP <u>Unassigned</u>
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U.S. PATENT DOCUMENTS													
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE							
													
FOREIGN PATENT DOCUMENTS													
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation							
						Yes	No						
													
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)													
	Digh Hisamoto et al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.												
	Yang-Kyu Choi et al., "Sub-20nm CMOS FinFET Technologies," 2001 IEEE, IEDM, pages 421-424.												
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	Yang-Kyu Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.												
EXAMINER 		DATE CONSIDERED 											

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).